

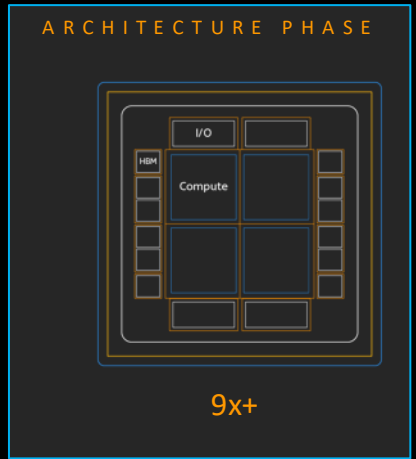
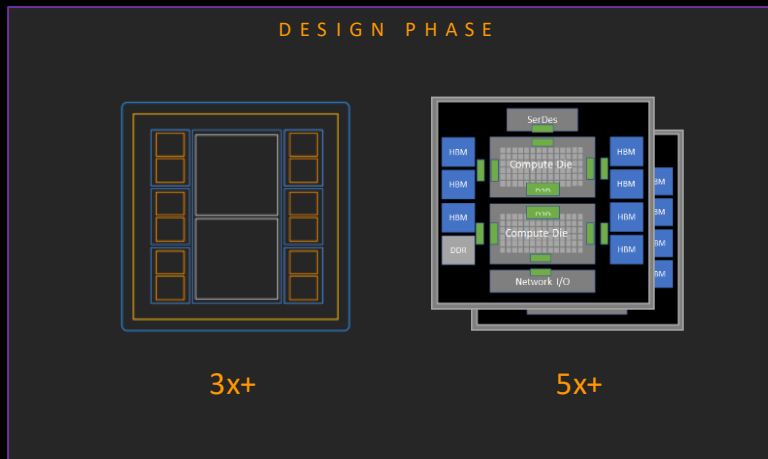
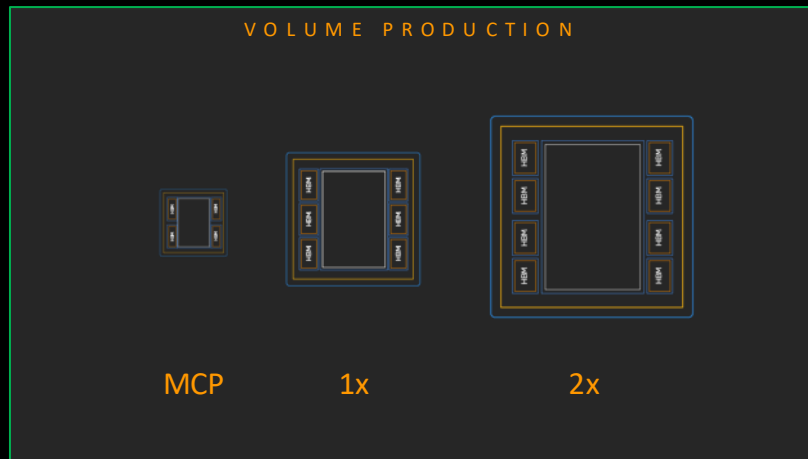
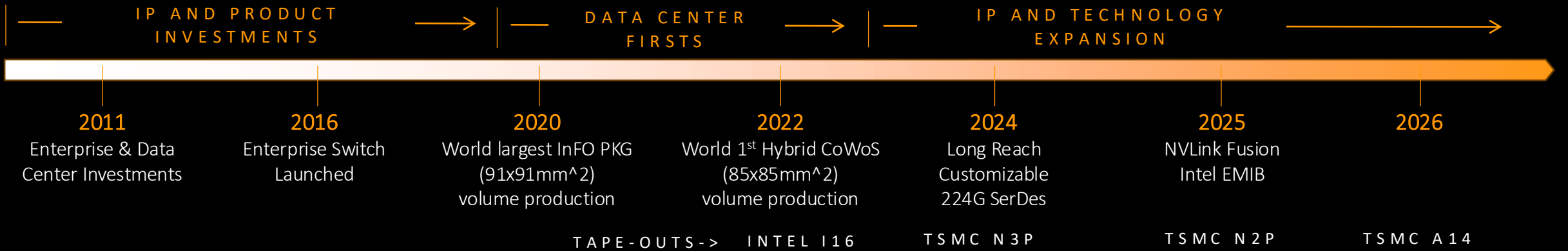


Data Center Solutions Overview

Anki Nalamalpu

VP & SENIOR GM –
DATA CENTER AND AI

Heritage of Innovation



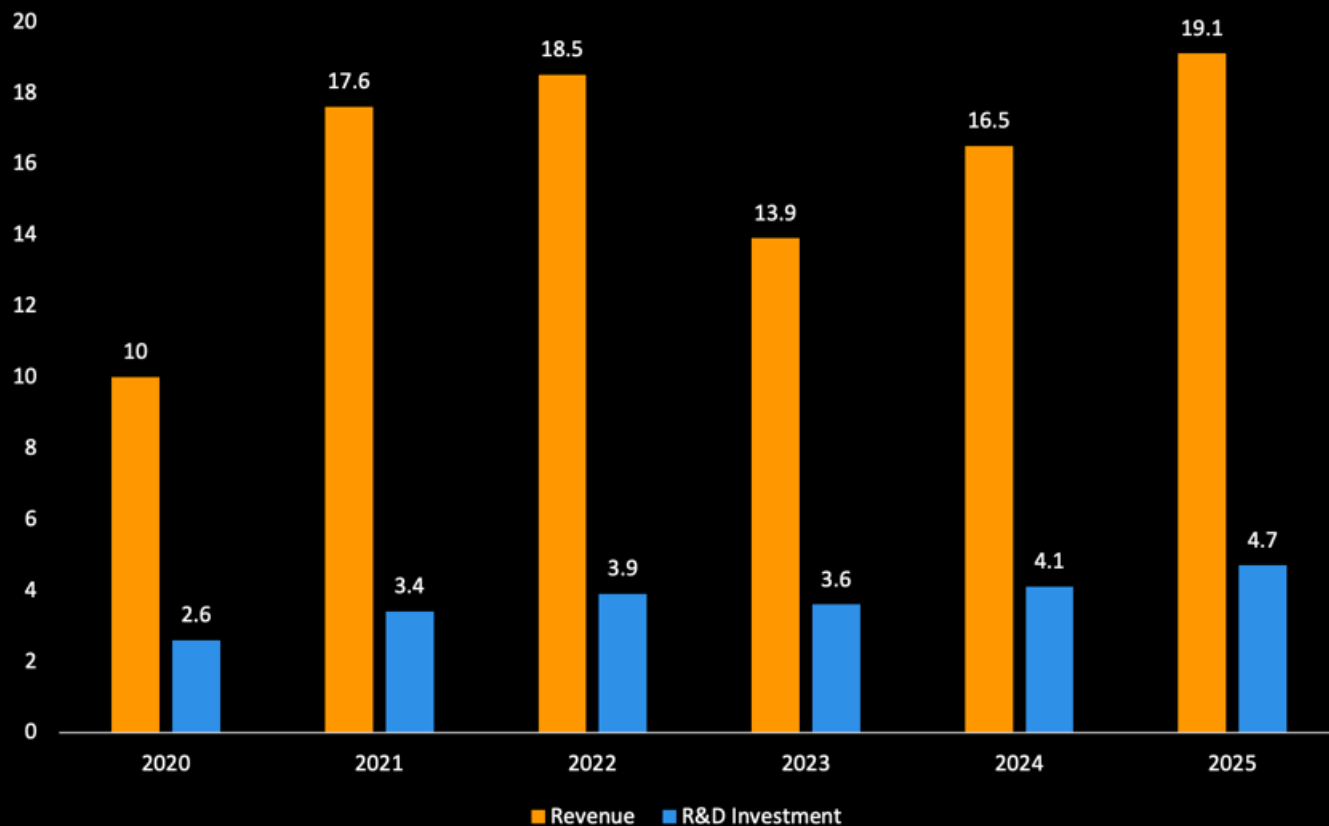
MediaTek Group Financials (USD \$B)

CONSISTENTLY
INVESTING

~25%

OF REVENUE
ON R&D

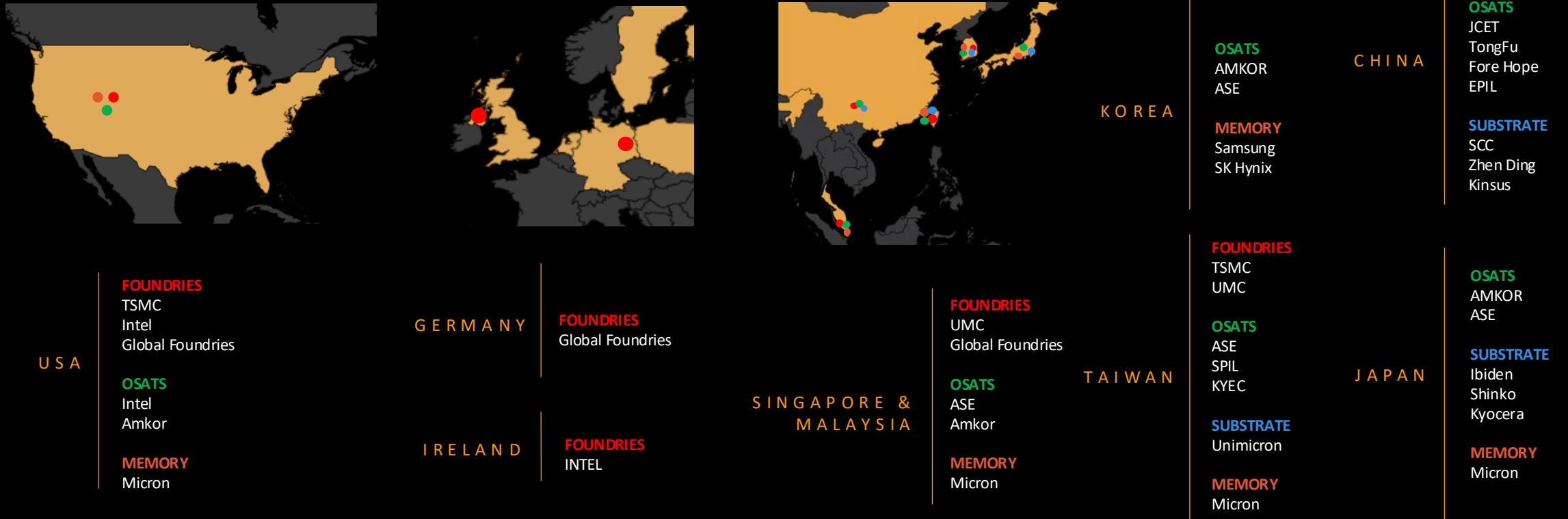
MEDIATEK **AIROHA** **RICHTEK**
(ETHERNET) (POWER IC)



Data Center Supply Chain Partnerships

Global Scale | Resiliency | Predictability | Leading-edge Technology

11 Foundries in 8 countries | 13 OSATS in 5 countries | 14 Substrate vendors in 4 countries | 3 Memory vendors in 5 countries



Map is not to scale. Areas shown are for guidance only – they are not precise locations

Strategic Partnerships with Industry Leaders

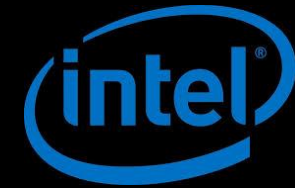
PRODUCT CO-DEVELOPMENT



Automotive | IoT | AI Supercomputer |
Data Center IP (NV Link)



EARLY TECHNOLOGY ENABLEMENT



Advanced Nodes | DTCO | CPO | SOW

- Early DTCO/STCO and 3DBlock partner
- Our collaboration has yielded worldclass D0 and capacity allocations
- Taped out IFS16 in 2024 and MP in 2025

Ongoing Research & Development



Next-gen Active Optical Cable (AOC) powered by MicroLED light sources and the MOSAIC architecture.

MediaTek and Microsoft proof-of-concept showcases:

- Dramatic power savings
- Copper-level reliability
- Extended reach for AI clusters
- Greater scalability

We're committed to further miniaturization and mass-production readiness for gigawatt-scale AI data centers.

The Rack

Building blocks of data centers

The new unit of compute consumption

Greater value through hardware/software vertical integration for Cloud AI and enterprise customer

Power, thermals and reliability dictate the performance

Effective monetization requires optimization of rack across different usages

Perf/TCO and Perf/Watt are critical metrics to achieve best-in-class data center efficiency

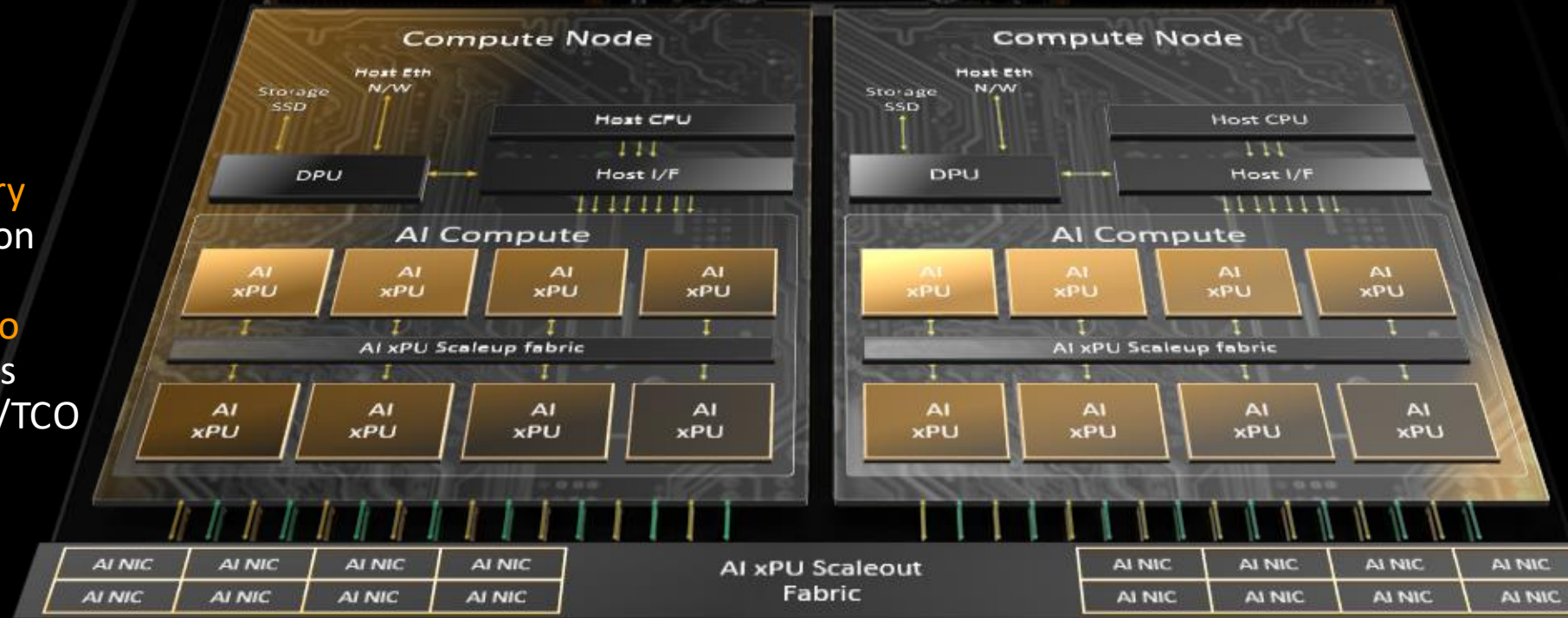


MediaTek Solutions to Scale Cloud Compute

Co-optimization across three pillars:
Compute, Scale-up, and Scale-out Interconnect

Supports industry standard (UALink, UEC) and proprietary interconnect (NVLink) solution

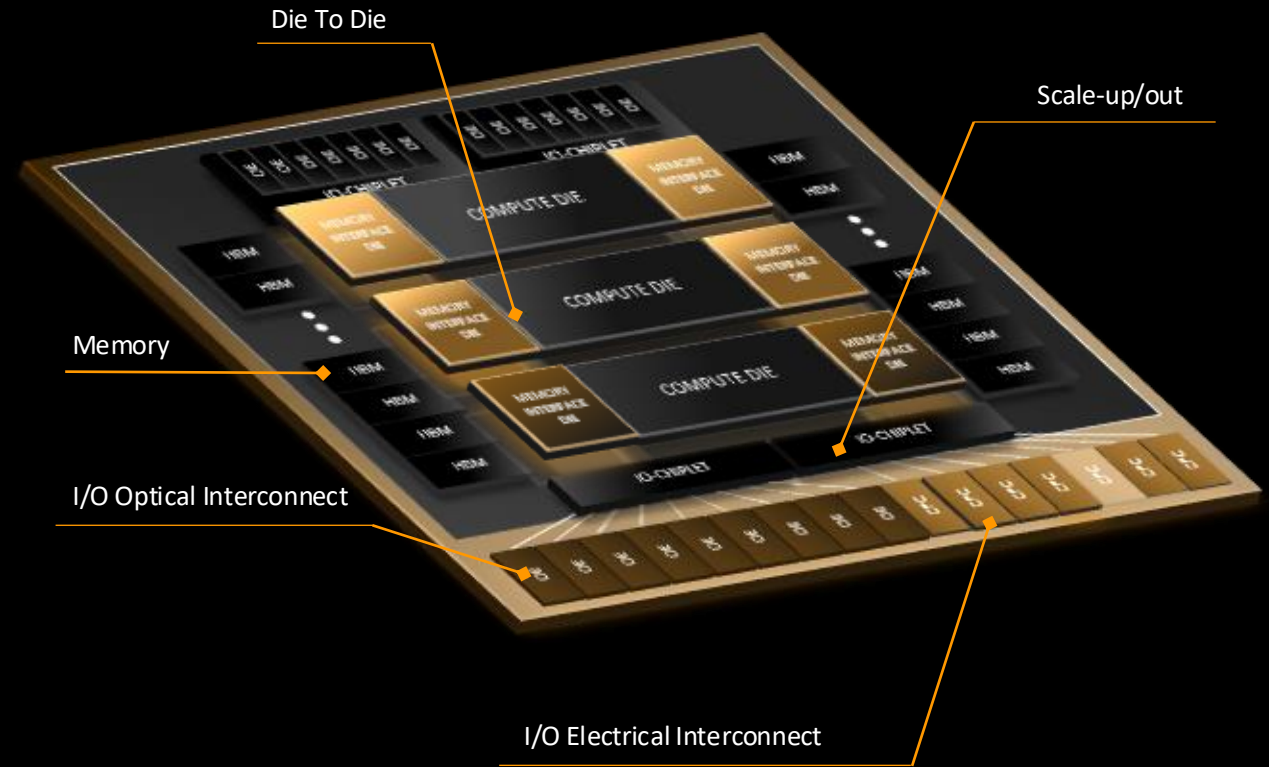
Heterogeneous integration to enable new system use-cases with improved performance/TCO



xPU

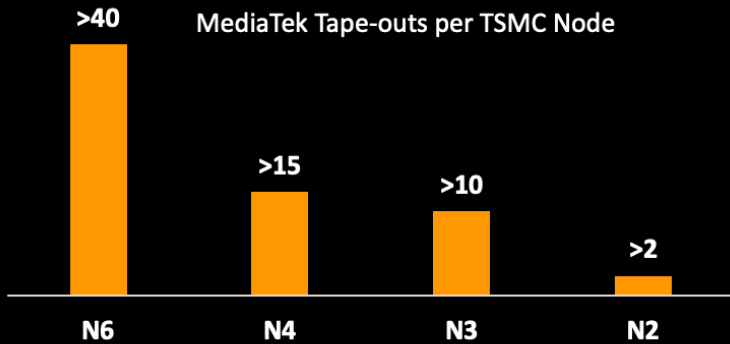
BETTER Perf/Watt and Perf/TCO
with LARGER and more COMPLEX
integrations

MediaTek is investing in technologies
and IPs to enable end to end
10x+reticle designs solutions



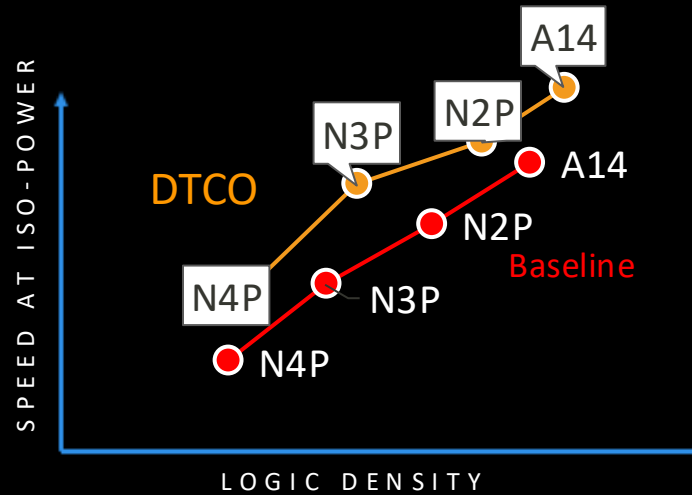
MediaTek Capabilities for Improving Compute Perf/W

EARLY NODE ADOPTION



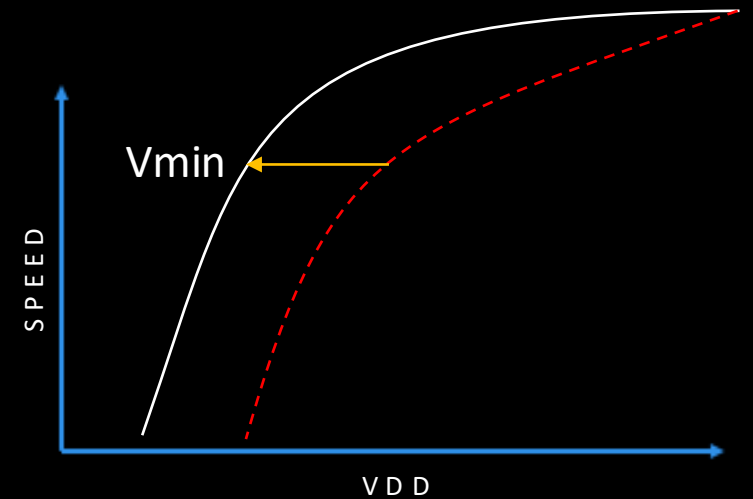
1st wave of 2nm tech adoption in 2025
A14 Test Chips in mid-2026

DTCO



Process entitlement with additional Design Technology Co-optimization (DTCO)

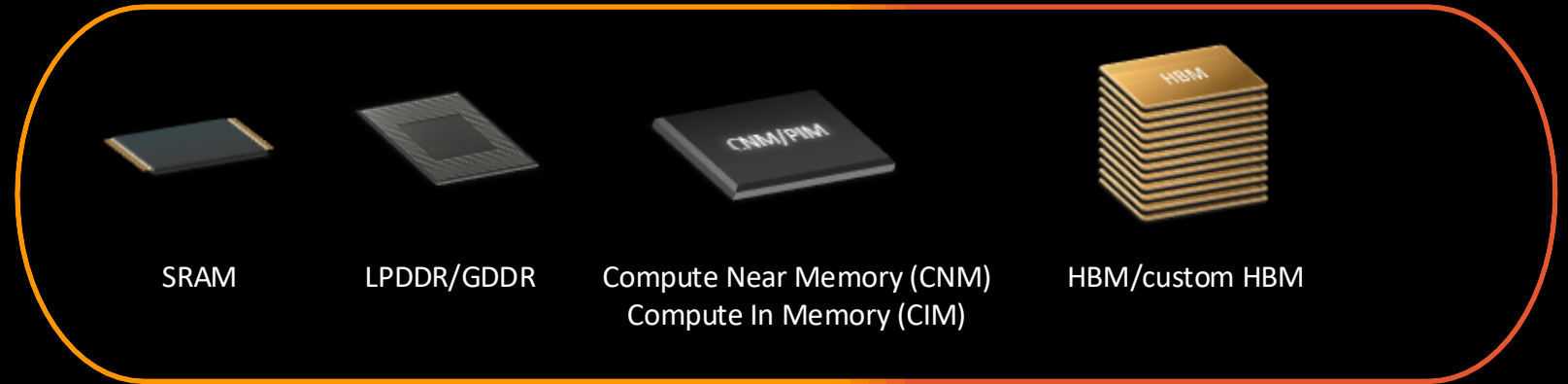
LOW VOLTAGE DESIGNS



Low Voltage designs for better Performance/Watt

Memory: A Critical Enabler For xPU

Training and inference specific memory innovations are critical for step jumps in performance



MediaTek memory solutions for xPU
Perf/W and Perf/TCO

- Extending world's best performing LPDDR solutions with DC capabilities
- Leading edge best in class custom SRAM solutions
- **Highest performance standard HBM**
- Custom HBM development

MediaTek Interconnect Technologies and IP

Interconnect solutions that span from die to rack for best in class perf, power and reach

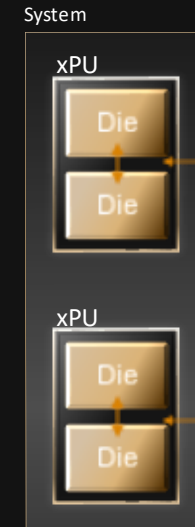
ON PACKAGE Die-to-die interconnect



TECHNOLOGY

- UClie
- Mlink

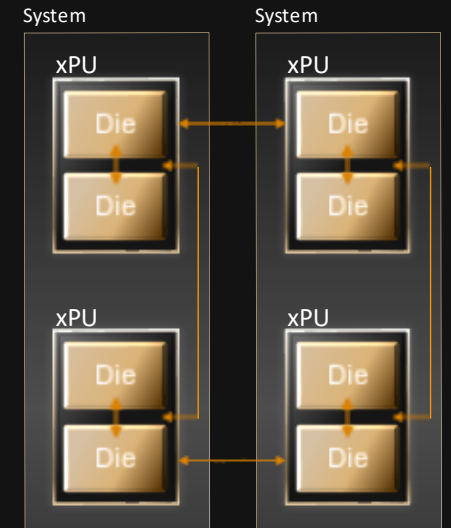
ON BOARD Chip-to-chip interconnect



TECHNOLOGY

- High-Speed SerDes (PCIe)
- uLED

OFF BOARD Board-to-board interconnect

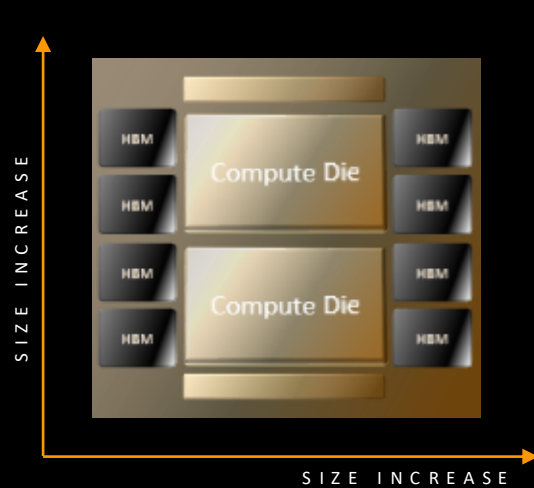


TECHNOLOGY

- High-Speed SerDes (Ethernet)
- NPC/CPC Connectors
- Co-Package Optics

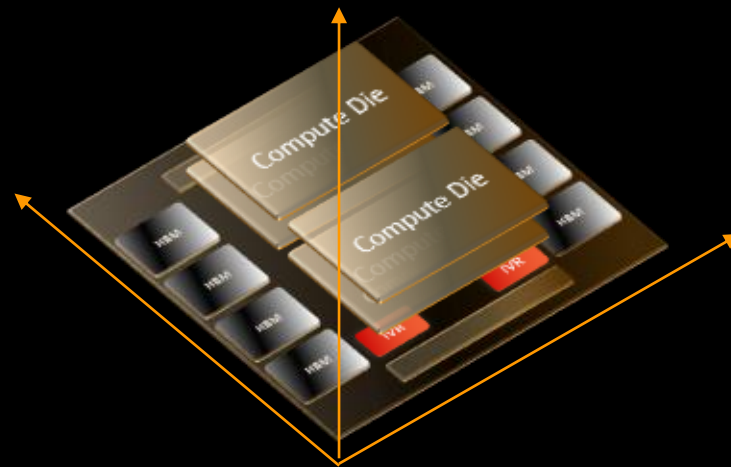
Advanced Packaging Technology Innovations

Critical for achieving larger integration



2.5D

< 10,000 sq. mm Si

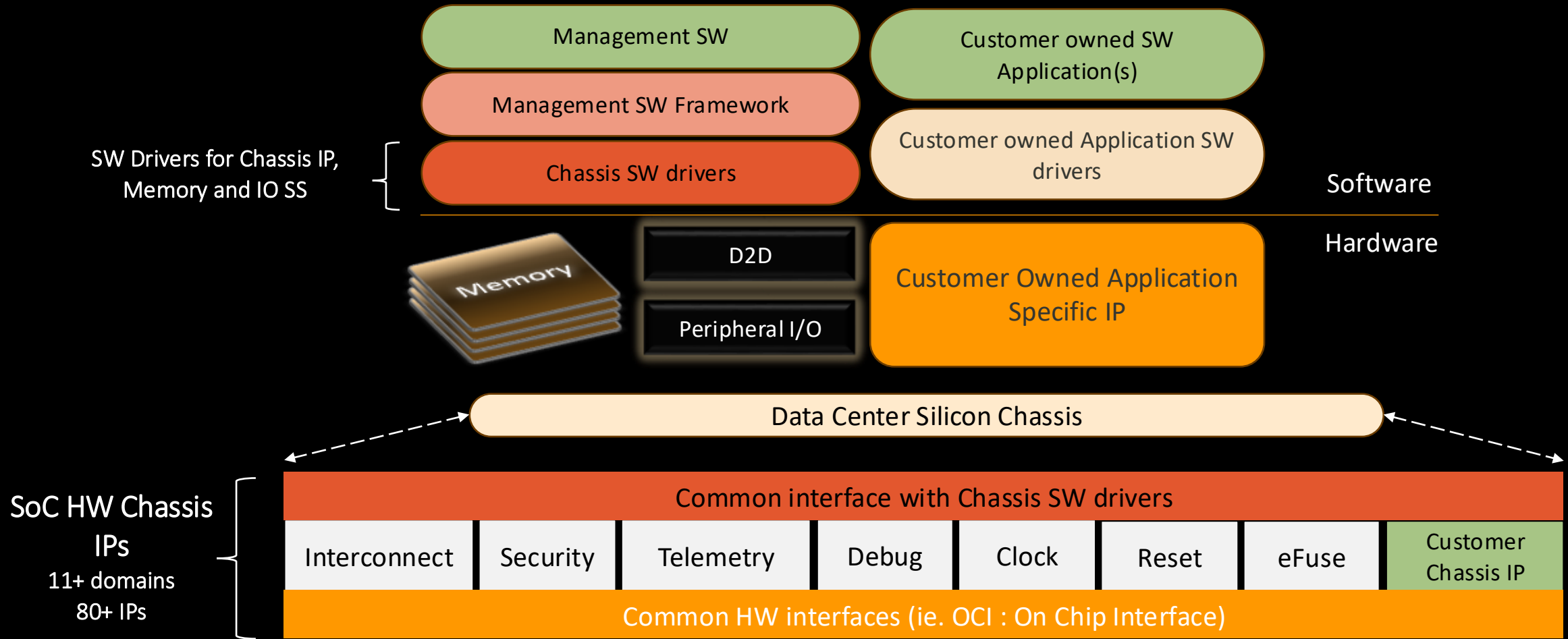


3.5D

10,000-20,000 sq. mm Si

- MediaTek's investments drive advanced packaging solutions to enable large complex heterogeneous integration.
- Advanced power delivery technologies (IVR, IPD) deliver higher power density and efficiency.
- System technology co-optimization (STCO) capabilities across Power Delivery, Thermals, Performance, and Packaging.

Datacenter SoC HW Chassis – XPU Shell



First Time Si Success and TTM Enabler

Data Center Technology Highlights

Leadership portfolio supported through our flexible business model

PROCESS & PACKAGING

- Advanced access to N2 and A14
- Proven DTCO leadership
- Roadmap to >9x reticle and >2KW
- 2.5D/3D/3.5D, InFO, CoWoS, EMIB

ARCHITECTURE

- Scalable systems architecture and STCO
- DC SoC chassis/shell for faster TTM
- Custom compute IP for inference workloads

IP PORTFOLIO

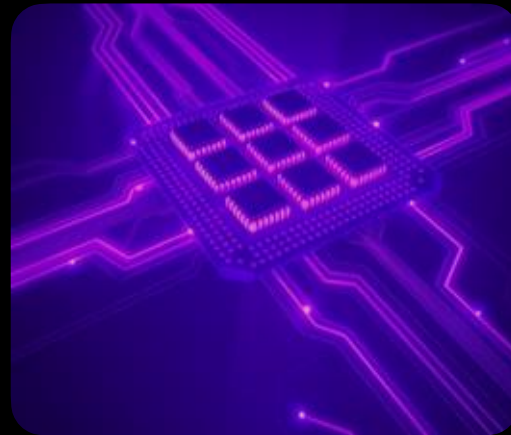
- Silicon-proven Ethernet, PCIe, memory subsystems
- Comprehensive 2.5D and 3.5D D2D solutions
- SerDes IP: 112/224/448G
- Interconnect solutions (Die to Rack)
- Standard and custom memory solutions
- Integrated Power Delivery (IVR, IPD)

The Value of MediaTek

Global
Scale

Technology
Optimization

Relentless
Execution



TECHNOLOGY LEADERSHIP

Process, Packaging,
Power, Connectivity

STRONG IP PORTFOLIO

SerDes, Optical,
High Speed I/O,
Die to Die Interconnect, Memory

COLLABORATIVE ECOSYSTEM

Partnerships & Global Supply Chain
TSMC, NVIDIA, Intel,
SK Hynix, Micron, Samsung

STRATEGIC ENGAGEMENT MODEL

Fast Time to Market
Flexibility Across the
Technology Lifecycle

MEDIATEK